

ABSTRACT

An analytical parasitic constraint generation technique for parasitic loading constraints generation based on analytical assessment of circuit nodes time constants. The inventive device includes DC operating point simulation, open circuit time constant calculator, circuit bandwidth estimation, parasitic loading constraints generator. DC operating point simulation calculates the equivalent resistive impedance at each circuit node. The time constant calculator analytically assesses the time constant related to each circuit node based on open-circuit time constant technique. Circuit bandwidth estimation module estimates the bandwidth of the circuit based on the calculated time constants at each node and then compares with band-width requirement. Parasitic loading constraints generator calculates the tolerable excessive parasitic loading at each circuit node to be used in physical synthesis, or to select optimal circuit topology.